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(54) **Organic semiconductor memory device having a MISFET structure and its control method.**

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PATENT ABSTRACTS OF JAPAN vol. 12, no. 488 (P-803) 20 December 88, & JP-A-63 200396

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Description

BACKGROUND OF THE INVENTION

[Field of the Invention]

This invention relates to a semiconductor memory device having a MISFET structure for information processing through a neural network and further to the control method thereof.

The semiconductor memory device herein mentioned refers to a device which shows non-linear electrical characteristics, i.e. those in electrical conductivity and capacity, depending on the energy of input, more specifically on its amount or change with time.

[Description of the Prior Art]

The information processing through a neural network, although a fine information processing performed in brains of living things, has so far been accompanied by a problem that there is no quality electronic device which functions like a synapse. This problem has confronted future information processing.

The neurochips having already been proposed can be classified into two types, semiconductor devices and optical devices. Although the neurochips using semiconductor devices have a more feasibility, they include no ones having appropriate characteristics for electronic devices having the plastic function. The result is that bipolar devices or CMOSs using a silicon semiconductor or the like are being improved as the devices performing analog operations for the development of a neural network.

On the other hand, the devices which are discussed for the one serving like a synapse to give the neural network a plastic function include the field-effect transistor (FET), transconductance amplifier (OTA), capacitor array, switched register, and so forth. Among them, the FET has excellent features such as low power and high gain, and those such as floating gates for EPROMs and MNOSs are attracting the eyes of the skilled in the art.

As for electrically conductive polymers, it is common knowledge that they are composed of polymers having large-extended conjugate π electron systems such as polyacetylene, polypyrrole, polythiophene, polyaniline, polyacene, and so forth, and contain electron donors (e.g. metal ions) or electron acceptors (anions such as Lewis acid or protonic acid) as a dopant, thus showing a high electrical conductivity. The resultant dopant, however, has had a large drawback that it will be diffused in a polymer matrix due to an electric field, thereby causing its conductivity to be varied.

Molecule-based transistors that have made use of the above drawback in turn are disclosed in Journal of American Chemical Society, 106, p.5375, 1984 edition by M.S. Wrighton et al., and ibid. 109, p.5526, 1987 edition by M.S. Wrighton.

Furthermore, an electrically conductive variable device intended for a plastic device is disclosed in Japanese Patent Laid-Open No. 63-200396.

However, the conventional devices described above have been unsatisfactory in that they have neither appropriate characteristics for an electronic device nor those for a plastic device.

It is therefore the primary object of this invention to provide a semiconductor memory device having high-gain high-performance characteristics using a novel electrical control device. Another object of this invention is to provide a control method for this semiconductor memory device.

This invention provides a semiconductor memory device having a MISFET structure comprising an electron conjugate polymeric semiconductor layer containing a mobile dopant for imparting electrical conductivity formed between a pair of electrodes and at least a first gate electrode provided between said pair of electrodes with an insulating layer or a high-resistance layer interposed along said electron conjugate polymeric semiconductor layer so that dopant distribution in said electron conjugated polymeric semiconductor layer is controlled by said first gate electrode to control the electrical conductivity of a conductive channel consisting of said electron conjugated polymeric semiconductor layer. A control method for the semiconductor memory device according to this invention, comprises the step of programming or resetting the memory device by applying a positive or negative voltage pulse to the first gate electrode to change the dopant distribution of said electron conjugate polymeric semiconductor layer, thereby varying the electrical conductivity thereof; reading said memory device by applying ground potential to said first gate electrode and applying a voltage between said pair of electrodes.

The semiconductor memory device of this invention can control the dopant distribution in the electron conjugate polymeric semiconductor layer or dopant retaining layer through the gate voltage, thereby varying the electrical conductivity of the electron conjugate polymeric semiconductor layer, capable of amplifying the current across a pair of electrodes (equivalent to source and drain of FET) to a large extent allowing them to be switched.

This semiconductor memory device, whose operation is equivalent to the FET operation of a dopant mobile semiconductor, has excellent memory type non-linear electrical characteristics practically usable as a plastic device. More precisely, in the semiconductor memory device of this invention, when a voltage is applied to the gate electrode, it will be subjected to a substantial change in channel impedance as the number of carriers due to field effect is affected

by the time-varying dopant concentration. This movement of the dopant is of a memory type and would never be done without gate electric field. Accordingly, when a network is formed of the plastic devices in accordance with this invention, a superior neural network with a high S/N ratio may be formed by virtue of a high change ratio in its channel impedance.

BRIEF EXPLANATION OF THE DRAWINGS

Figs. 1 and 2 are sectional conceptual views each showing an example of a semiconductor memory device in accordance with this invention;
Fig. 3 is a view typically showing the movement of anion dopant when a p-type electron conjugate polymeric semiconductor is used;
Figs. 4 and 5 are views showing the equivalent circuit of the device in accordance with this invention and the correlation and principle of the device configuration;
Figs. 6 and 7 are views each showing an example of the construction of four and two terminals, respectively, in the device of this invention;
Fig. 8 is a chart showing the drain current response corresponding to gate voltages of the semiconductor memory device of this invention;
Fig. 9 is a chart showing the drain current-gate voltage (I_D-V_G) of the device of this invention; and
Fig. 10 is a view showing an example of the neural network of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 shows a sectional conceptual view illustrating an example of a semiconductor memory device of this invention. On a substrate 7, there is formed an electron conjugate polymeric semiconductor layer 3 containing a dopant, whereon are provided a pair of electrodes 1 and 2, and at least one gate electrode 5 is provided between the pair of electrodes 1 and 2 with an insulating layer 6 interposed.

For the material of the electron conjugate polymeric semiconductor layer 3, polythiophene, polypyrrole, poly-p-phenylene, and their copolymers and derivatives are used.

The electron conjugate polymer for this purpose is preferably supplied by synthesis through electrolytic polymerization (anodic oxidation polymerization or cathodic reduction polymerization) and a polymer derived from chemical polymerization may also be used.

Anodic oxidation polymerization is that a dopant is dissolved into an electron conjugate monomer solution and, under an electric field generated between at least one pair of electrodes, the electron conjugate monomer is electrolytically polymerized onto the anode with the result of obtaining an electrically conductive polymer into which the dopant has been dispersed.

This method enables a molecular order film to be formed easily and uniformly, thereby facilitating the constructing of high-speed responsive devices.

Furthermore, if both the dopant, imparting electronic conductivity, and the plasticizer dissolving the dopant are dispersed into a polymer having long π electron conjugate principal chains, an electron conjugate polymeric semiconductor layer having a high level of dopant mobility can be obtained, hence a semiconductor memory device having a high speed response.

Referring now to the operation of this invention, when a current source is connected across the electrodes 1 and 2, and a gate voltage to be applied to the gate electrode 5 is controlled, the channel impedance in the electron conjugate polymeric semiconductor layer 3 between the electrodes 1 and 2 will be controlled by the gate voltage. That is, the dopant concentration in the electron conjugate polymeric semiconductor layer 3 will be varied correspondingly to the gate voltage, thereby the channel impedance to be varied.

The channel impedance across the source and the drain of this semiconductor memory device is dependent on the dopant concentration in the channel (equivalent to the impurity concentration of a semiconductor), so that the lower the impedance, the more the drain current. An electron conjugate polymeric semiconductor features in that the electrical conductivity thereof will be greatly varied from insulator to conductor depending on its dopant concentration. The present invention is intended to exert this feature of the electron conjugate polymeric semiconductor to the best use.

The dopant in this invention is mobile and its polarity is reverse to that of the charge carriers of the electron conjugate polymeric semiconductor, so that the electrical conductivity of the channel will be largely varied in the reverse direction against the variation of conduction due to the FET principle. In addition, it is also possible that the mobility of the dopant has exact threshold values through the selecting of dopant, i.e. its ion radius and the amount of electric charge.

Fig. 8 illustrates the operation characteristics showing the drain current response corresponding to the gate voltage in the case where a p-type electron conjugate polymeric semiconductor and an anion dopant are used for the semiconductor memory device as an example. This figure is taken from a case in which the pulse width is longer than the movement of the dopant, where the gate voltage is varied to the three steps, a positive pulse voltage, a negative pulse voltage, and ground voltage. The response of field effect is in the order of microseconds, and the movement of dopant is in the order of milliseconds.

The state of the operation of this device can be represented as in Fig. 9 from the viewpoint of I_D-V_G

characteristic, equivalent to such a characteristic just as MOSFETs of enhancement type and depression type are combined.

Using this semiconductor memory device, when a semiconductor memory device 13 is connected in a network shape as shown in Fig. 10, and subjected to a learning with a positive gate pulse and a reset with a negative gate pulse as shown in Fig. 8, only the device in the network subjected to the learning results in an extremely low impedance, thus a neural network being formed up. This device, although taking a time in the order of milliseconds for the learning and the reset, features in allowing its conduction after the learning to respond in microseconds. Accordingly, although the learning and the reset of the semiconductor memory device take milliseconds for response, the operation thereof as a neural network makes use of the electronic conductivity of the channel so that the device can operate in microseconds or lower.

As will be understood from the above description, the device of this invention is a semiconductor device having an excellent plasticity with a substantially large variation in electrical conductivity, usable for information processing through a neural network.

Moreover, when a plurality of such semiconductor memory devices are used in connection as shown in Fig. 10, IC devices can be constructed in the same manner as in semiconductor integrated circuit process, thereby allowing a neural network to be constructed on a chip and hence a large contribution toward information processing.

Fig. 2 shows an example of the semiconductor memory device with a higher performance having been formed up by overlaying a mobile dopant retaining layer 4 and an electron conjugate polymeric semiconductor layer 3 onto an electrically conductive substrate 8.

The mobile dopant retaining layer 4 is a layer so constructed as to allow the dopant easily to move, therefore being preferably of a low conductivity. The layer may also be an electrically conductive anisotropic film having a high insulating characteristic in the direction of the layer and a high conductivity in the orthogonal direction thereof.

In the device represented in Fig. 2, due to the movement of the dopant under the electric field, ion radicals of the inverse polarity to that of the dopant occur in the electron conjugate polymer into which the foregoing dopant has penetrated. On the other hand, ions of the inverse polarity remaining in the dopant retaining layer 4 will undergo a redox. The dopant retaining layer 4, therefore, must be of a substance being reversible and stable against the redox. The construction above mentioned can make reversible and stable this electrical redox in the dopant retaining layer 4 which occurs during the operation of the gate electrode. When the ion radical is an electron donor (D), ($D^{\cdot+} + e^- \rightleftarrows D^0$) is steadily repeated, while, when an electron acceptor, ($A^{\cdot-} \rightleftarrows A + e^-$) is steadily repeated. For a p-type electron conjugate polymer, anion dopant is doped by the gate electrode thereby increasing the electrical conductivity thereof, with + charges of cationic radicals remaining in the dopant retaining layer 4. These charges are then reduced by the electrons from the inverse electrode, returning to neutral. And vice versa for an n-type polymer. Thus, in the dopant retaining layer 4 the redox reaction is reliably repeated.

The mobile dopant retaining layer 4 is formed of a layer made up by dissolving into an ionic polymer a dopant primarily comprising electron donors (metal ions or the like) or electron acceptors (anions such as Lewis acid and proton acid), the layer is also an ion conductive polymeric compound. It is preferable that the mobile dopant retaining layer 4 comprises a polymer complex layer formed of a dopant and a polymer, in which the mobility of the dopant may have exact threshold values, this case including ionic clathrate compounds or polyion complexes.

For the clathrate compounds, a polymer having an alkylene oxide construction such as crown either or polyethylene oxide is appropriate, while the polymers used for the polyion complexes include polymers containing amino groups, polyurethane, polyamide, polyacrylic acid, polyester, and other like polar polymers.

For the mobile dopant retaining layer 4, the construction utilizing an ion radical contained polymeric compound including a mobile dopant is the simplest and preferred in practice, while the ion radical of the inverse polarity to the dopant is preferably of immobility, i.e. an ion radical of a high bulky molecular weight.

This ion radical contained polymer compound including the mobile dopant comprises at least one of the following types:

(a) a low-conductivity electron conjugated polymeric compound containing a mobile dopant, (b) a polymeric compound into which a salt out of a mobile dopant and an inversely charged ion radical is dispersed, (c) a polymeric complex formed of a mobile dopant and an ion radical polymer, and (d) a low-conductivity compound formed of a mobile dopant contained high-conductivity electron conjugated polymer and an insulating polymer, each of which is detailed below:

(a) The low-conductivity electron conjugated polymeric compound containing a mobile dopant comprises a polymer having π electron conjugated side chains or that including no long-distance electron conjugated main chain, which includes numerous low-conductivity polymers such as, specifically, phenyl-substituent polyacetylene, thiophene copolymer, pyrrole copolymer, and polyvinyl carbazole.

(b) The polymeric compound into which a salt made of a mobile dopant and an inversely

charged ion radical is dispersed has such a structure that a salt having, as ion radicals, heterocyclic cation radicals containing nitrogen and/or sulfur or anion radicals such as haloquinone and cyanoquinone has been molecularly dispersed into a compatible polymer, the construction being possible obtained by a large number of charge-transfer type organic semiconductor molecularly dissolved in a polar polymer. for this polar polymer, a polymer containing nitrogen or sulfur is suitable, specifically such as an amino-group contained polymer, polyurethane, polyamide, and polyester.

(c) The ion radical polymer here used may be either a cation radical polymer or an anion radical polymer, whereas a cation radical polymer having in its side chains or main chains heterocyclic cation radicals containing nitrogen and/or sulfur is the most conveniently available, such as polymers containing pyridine rings, pyrimidine rings, triazine rings, imidazole rings, thiazole rings, thiopyran rings, thiophene rings, pyrrole rings, indole rings, and quinoline rings.

(d) For the low-conductivity compound made of a mobile dopant contained high-conductivity electron conjugated polymer and an insulating polymer, such a compound with an arbitrary electrical conductivity may simply be derived by compounding an electron conjugate polymer containing the dopant with a high conductivity and an insulating polymer.

Fig. 3 typically illustrates the movement of the dopant within the semiconductor memory device in Fig. 2, wherein on an electron conjugate polymeric semiconductor layer 3 including p-type electron conjugate polymeric semiconductor 9, 9-1 and anion dopant 10 there is provided a gate electrode 5 therebetween with an insulating layer interposed. The anion dopant 10 in this invention is mobile and moreover has the polarity opposite to that of the p-type electron conjugate polymeric semiconductor 9, 9-1, so that the dopant will move in the direction of the layer thickness correspondingly to the voltage applied to the gate electrode, thus the channel impedance being subjected to a considerable change by the effect of the movement of the anion dopant 10. This moving speed of the dopant can be determined depending on the amount of charge, ion radius, type of polymer, density, internal viscosity, temperature, and the like of the dopant.

The equivalent circuit and principle of such a device in accordance with this invention are shown in Figs. 4 and 5. Fig. 5 depicts an example of the device construction wherein the insulating layer 6 at the gate in Fig. 4 is replaced by a high resistance layer 6-1 having a low insulation resistance. The high-resistance layer 6-1 at the gate is preferably made from a material having an electrical resistivity of 10^5 to 10^{12} Ω·cm. It is furthermore necessary that the electrical conductivity of the electron conjugate polymeric semiconductor layer 3 between a pair of electrodes after doping be markedly higher than that of the mobile dopant retaining layer 4, as is apparent from the equivalent circuit shown here. The device in accordance with this invention is characterized by its capability of forming a high-gain device making use of its feature that the electrical conductivity of the conductive polymer will widely vary up to a range of 10 orders of magnitude in the direction of the film, i.e., that of source to drain. On the other hand, the device will allow a high strength of electric field to be applied in the thickness direction, thereby rendering the response speed faster.

Although Fig. 3 shows, for the sake of explanation, only an example utilizing the p-type electron conjugate polymeric semiconductor layer 9, 9-1 and the anion dopant 10, it will be apparent to the skilled in the art that this invention is not limited to this example and this is the case also when cation dopant is doped into an n-type electron conjugate polymeric semiconductor.

The semiconductor memory device of this invention may be constructed not only with three terminals but also with four terminals, for example, taking a substrate terminal using silicon single crystal having an SiO_2 insulating surface. In this case, the control characteristic thereof will be of a higher precision and bistable.

Fig. 6 illustrates an example of the four-terminal device, wherein the four-terminal semiconductor memory device is so constructed that on a gate electrode 11 comprising a semiconductor substrate having an insulating film 6 on its surface there is provided an electron conjugate polymeric semiconductor layer 3 and a mobile dopant retaining layer 4 are overlaid with a dopant penetrating separation layer 12 interposed therebetween.

The dopant penetrating separation layer 12 interposed between the electron conjugate polymeric semiconductor layer 3 and the dopant retaining layer 4 serves to accurately control the dopant distribution, thereby stabilizing the switching current between a pair of electrodes. For this dopant penetrating separation layer 12, an ion penetrating porous film or the like may be used; for example, a separator material is suitable therefor.

At both ends of the electron conjugate polymeric semiconductor layer 3 and the dopant retaining layer 4 there are provided electrodes 1 and 2. On the mobile dopant retaining layer 4 there is provided a gate electrode 5 with a high-resistance layer 6-1 interposed therebetween. A drive power supply is connected between the electrodes 1 and 2.

A control voltage in the form of pulse voltage is applied to each of gate electrodes 5 and 11, and the dopant distribution will accurately be controlled by controlling the amount, phase, and the like of the

pulse voltage for both electrodes.

This invention may also be constructed for a two-terminal plastic device such as shown in Fig. 7, wherein the gate electrode 5 is short-circuited with one of the pair of electrodes 1 and 2, e.g. with the source electrode 1, and a positive or negative pulse voltage is applied between the pair of electrodes 1 and 2 to control the dopant distribution in the electron conjugate polymeric semiconductor layer 3 or the dopant retaining layer 4, thereby varying the electrical conductivity for learning or reset operation, while a voltage lower than the pulse voltage is applied between the pair of electrodes 1 and 2 for driving into conduction.

As described hereinabove, the semiconductor memory device of this invention is bistable and performs switching in connection with time and the amount of current, thus being useful for artificial intelligence devices (neurochips). If IC devices are formed in the same manner as in the semiconductor integrated circuit process using a plurality of such semiconductor memory devices, neuronetwork devices can easily be formed up.

Now the invention will be described with reference to several embodiments.

Example 1

As shown in Fig. 2, on an electrically conductive substrate 8, there were formed a 5 μm thick dopant retaining layer 4 and an electron conjugate polymeric semiconductor layer 3 comprising a 10 μm thick polythiophene layer by overlaying them, where a pair of electrodes 1 and 2 were provided thereon and a gate electrode 5 was provided therebetween with an insulating layer 6 interposed. For the dopant retaining layer 4, a perchlorate derived from a copolymer of 2-vinylpyridine and vinyl acetate was used. Thus, a semiconductor memory device was obtained.

When a pulse voltage was applied to the gate electrode 5 of this device into operation, the device has shown such non-linear switching characteristics as shown in Fig. 9. Making use of this operation, the device may be subjected to a learning with a positive gate pulse and be reset with a negative pulse, as shown in Fig. 8.

With this device in use for forming up the neural network shown in Fig. 10, when a voltage was applied across an arbitrary pair of I/O terminals, only the portion of the device along the shortest course from the input terminal to the output terminal resulted in an extremely low impedance, so that the device could experience the learning of the relation between the input and output as a change in the resistivity thereof.

Example 2

As shown in Fig. 7, on an electrically conductive substrate 8, there were formed a 20 μm thick dopant retaining layer 4 and a 10 μm thick electron conjugate polymeric semiconductor layer 3 by overlaying them one after another, where a pair of electrodes 1 and 2 and an insulating layer 6 were formed thereon and a gate electrode 5 was provided further thereon, thus constructing a semiconductor memory device. For the mobile dopant retaining layer 4, a perchlorate derived from a copolymer of 4-vinylpyridine and vinyl acetate was used. In the semiconductor memory device thus obtained, the gate electrode 1 thereof was short-circuited with the source electrode 1 so as to make the device experience a learning with a positive gate pulse of 10 V and reset with a negative gate pulse of 10 V, so that it has shown a change of up to 10^6 of the channel impedance.

With this device in use for forming up the neural network shown in Fig. 10, when a voltage was applied across an arbitrary pair of I/O terminals, only the portion of the device along the shortest course from the input terminal to the output terminal resulted in an extremely low impedance, so that the device could experience the learning of the relation between the input and output as a change in the resistivity thereof.

Example 3

As shown in Fig. 2, on an electrically conductive substrate 8, there were formed a 6 μm thick dopant retaining layer 4 and an electron conjugate polymeric semiconductor layer 3 comprising a 11 μm thick polypyrrole layer by overlaying them, where a pair of electrodes 1 and 2 were formed thereon and a control electrode 5 was provided therebetween with an insulating layer 6 interposed. For the mobile dopant retaining layer 4, polydiphenyl acetylene was used. The electrically control device thus obtained, when put into operation, has shown such a switching characteristics as in Fig. 9.

Example 4

As shown in Fig. 7, on an electrically conductive substrate 8, there were formed a 10 μm thick dopant retaining layer 4 and an electron conjugate polymeric semiconductor layer 3 comprising a 8 μm thick polypyrrole layer by overlaying them, where a pair of electrodes 1 and 2 and an insulating layer 6 were formed thereon and a control electrode 5 was further provided on the insulating layer. and the control electrode 5 was short-circuited with the source electrode 1 with a resistor, thus constructing a two-terminal electrically control device. For the mobile dopant retaining layer 4, a polyvinyl chloride compound in which a 30% perchlorate of 2,3,4,5-tetra-(4-pyridine) thiophene was dispersed was used. With the electrically control device thus obtained in use for forming up a nonlinear resistive neuro network, when the device was put into

operation, a network having a resistance pattern corresponding to the learning signals could be created.

Example 5

As shown in Fig. 6, on a silicon substrate 11 including an oxidized insulating film 6, there were formed a 5 μm thick dopant retaining layer 4 and an electron conjugate polymeric semiconductor layer 3 comprising a 10 μm thick polypyrrole layer by overlaying them with a dopant penetrating separation layer 12 interposed therebetween, where a pair of electrodes 1 and 2 and a high-resistance layer 6-1 were provided thereon and a control electrode 5 was further provided on the high-resistance layer, thus constructing an electrically control device. For the mobile dopant retaining layer 4, a compound of polyvinyl quinoline tetraborate and urethane was used. The electrically control device thus obtained, when put into operation, has shown switching characteristics and source-drain current time-characteristics similar to that of Example 1.

Claims

1. A semiconductor memory device having a MISFET structure comprising an electron conjugate polymeric semiconductor layer (3) containing a mobile dopant for imparting electrical conductivity formed between a pair of electrodes (1, 2) and at least a first gate electrode (5) provided between said pair of electrodes (1, 2) with an insulating layer (6) or a high-resistance layer interposed along said electron conjugate polymeric semiconductor layer (3) so that dopant distribution in said electron conjugated polymeric semiconductor layer (3) is controlled by said first gate electrode (5) to control the electrical conductivity of a conductive channel consisting of said electron conjugated polymeric semiconductor layer.

2. A semiconductor memory device as claimed in claim 1,
wherein the electron conjugate polymeric semiconductor layer (3) comprises a dopant for imparting electrical conductivity, a polymer having a long π electron conjugate main chain, and a plasticizer dissolving said dopant.

3. A semiconductor memory device as claimed in claim 1,
wherein the electron conjugate polymeric semiconductor layer (3) is of at least one type selected out of electrolytically polymerized polythiophene, polypyrrole, poly-p-phenylene, and their copolymers and derivatives.

4. A semiconductor memory device as claimed in claim 1,
wherein the electron conjugate polymeric semiconductor layer (3) is formed adjacent to a dopant retaining layer (4) consisting of a polymeric compound layer complexed with said mobile dopant or of an ion radical contained polymeric compound including said mobile dopant.

5. A semiconductor memory device as claimed in claim 4,
wherein the ion radical contained polymeric compound comprises at least one type selected out of
(a) a low-conductivity electron conjugated polymeric compound containing a mobile dopant,
(b) a polymeric compound in which a salt derived from a mobile dopant and an inverse-polar ion radical is dispersed,
(c) a polymer complex of a mobile dopant and an ion radical polymer, and
(d) a low-conductivity compound made of a mobile dopant contained high-conductivity electron conjugate polymer and an insulating polymer.

6. A semiconductor memory device as claimed in claim 5,
wherein the dopant contained low-conductivity electron conjugated polymeric compound comprises a polymer having π electron conjugated side chain or a polymer having no long-distance electron conjugate main chain thereof.

7. A semiconductor memory device as claimed in claim 5,
wherein the polymeric compound into which a salt made of a mobile dopant and a reverse-polar ion radical is dispersed comprises a salt having, as ion radicals, heterocyclic cation radicals containing nitrogen and/or sulfur or anion radicals such as haloquinone and cyanoquinone has been molecularly dispersed into a compatible polymer.

8. A semiconductor memory device as claimed in claim 5,
wherein the ion radical polymer is a polymer having heterocyclic cation radicals containing nitrogen and/or sulfur in its side chain or main chain.

9. A semiconductor memory device as claimed in claim 4,
wherein the polymeric compound layer forms an ion clathrate compound or a polyion complex with a mobile dopant.

10. A semiconductor memory device as claimed in claim 9,

wherein the ion clathrate compound is of a construction of crown ether or polyethylene oxide.

11. A semiconductor memory device as claimed in claim 4,
wherein the electron conjugate polymeric semiconductor layer (3) and the dopant retaining layer (4) are separated by a dopant penetrating layer.

12. A semiconductor memory device as claimed in claim 11,
wherein said first gate electrode (5) is formed on said dopant retaining layer (4) with said insulating layer (6-1) interposed therebetween, and a second gate electrode (11) is provided on said electron conjugate polymeric semiconductor layer (3) with an insulating layer (6) interposed therebetween.

13. A semiconductor memory device as claimed in claim 12,
wherein the second gate electrode (11) is a semiconductor substrate.

14. A semiconductor memory device as claimed in any of claims 1 to 13,
wherein the first gate electrode (5) is short-circuited with one of said pair of electrodes (1, 2).

15. A control method for the semiconductor memory device according to claims 1 to 13,
comprising the step of programming or resetting the memory device by applying a positive or negative voltage pulse to the first gate electrode to change the dopant distribution of said electron conjugate polymeric semiconductor layer, thereby varying the electrical conductivity thereof; reading said memory device by applying ground potential to said first gate electrode and applying a voltage between said pair of electrodes.

16. A control method for the semiconductor memory device according to claim 14,
comprising the steps of programming or resetting the memory device by applying a positive or negative voltage pulse between said pair of electrodes to change the dopant distribution of said electron conjugate polymeric semiconductor layer, thereby varying the electrical conductivity thereof; reading said memory device by applying a voltage between said pair of electrodes having a smaller amplitude than that of said voltage pulse.

Patentansprüche

1. Halbleiter-Speicherbauelement mit einer MISFET-Struktur mit einer elektronenkonjugiert-polymerischen Halbleiterschicht (3), welche einen beweglichen Dotierstoff zum Einbringen elektrischer Leitfähigkeit, welche zwischen einem Elektrodenpaar (1, 2) und mindestens einer ersten Gate-Elektrode (5) gebildet wird, welche zwischen einem Elektrodenpaar (1, 2) vorgesehen ist, mit einer Isolierschicht (6) oder einer entlang der elektronenkonjugiert-polymerischen Halbleiterschicht (3) dazwischengelegten hochohmigen Schicht, so daß die Dotierstoffverteilung in der elektronenkonjugiert-polymerischen Halbleiterschicht (3) durch die erste Gate-Elektrode (5) gesteuert werden kann, um die elektrische Leitfähigkeit eines leitenden Kanals zu steuern, der aus der elektronenkonjugiert-polymerischen Halbleiterschicht besteht.

2. Halbleiterspeicherbauelement nach Anspruch 1, in dem die elektronenkonjugiert-polymerische Halbleiterschicht (3) einen Dotierstoff zum Einbringen elektrischer Leitfähigkeit, ein einen langen π-elektronenkonjugierten Hauptstrang aufweisendes Polymer und einen Weichmacher, welcher den Dotierstoff herauslöst, beinhaltet.

3. Halbleiterspeicherbauelement nach Anspruch 1, in dem die elektronenkonjugiert-polymerische Halbleiterschicht (3) aus mindestens einem Stoff besteht, ausgewählt aus elektrolytisch polymerisiertem Polythiophen, Polypyrrol, Poly-P-Phenyl und deren Kopolymere und Derivate.

4. Halbleiterspeicherbauelement nach Anspruch 1, in dem die elektronenkonjugiert-polymerische Halbleiterschicht (3) benachbart zu einer dotierstoffzurückhaltenden Schicht (4) angeordnet ist, welche aus einer polymerischen Verbundschicht besteht, welche komplexbildend mit dem beweglichen Dotierstoff versehen ist, oder aus einem Ionenradikale enthaltenden polymerischen Verbund, einschließlich des beweglichen Dotierstoffes, gebildet ist.

5. Halbleiterspeicherbauelement nach Anspruch 4, in dem der Ionenradikale enthaltende polymerische Verbund mindestens einen der nachfolgenden Stoffe enthält:
   (a) einen schlecht leitfähigen einen beweglichen Dotierstoff enthaltenden elektronenkonjugiert-polymerischen Verbund,
   (b) einen polymerischen Verbund, in dem ein von einem beweglichen Dotierstoff und einem invers-polaren Ionenradikal abgeleitetes Satz verteilt ist,
   (c) einen Polymerkomplex aus einem beweglichen Dotierstoff und einem Ionenradikal-Polymer, und
   (d) einen schlecht leitfähigen Verbund aus ei-

nem ein hochleitfähiges elektronenkonjugiertes Polymer enthaltenen beweglichen Dotierstoff und einem isolierenden Polymer.

6. Halbleiterspeicherbauelement nach Anspruch 5, in dem der Dotierstoff enthaltende, schlecht leitfähige elektronenkonjugiert-polymerische Verbund ein Polymer mit einem π-elektronenkonjugierten Seitenstrang beinhaltet oder ein Polymer mit einem Hauptstrang desselben ohne langreichweitige Elektronenkonjugation.

7. Halbleiterspeicherbauelement nach Anspruch 5, in dem der polymerische Verbund, in dem ein aus beweglichem Dotierstoff und einem invers-polaren Ionenradikal gebildetes Salz verteilt ist, ein Salz enthält mit heterozyklische Kationenradikalen als Ionenradikale, welche Stickstoff und/oder Schwefel oder Anionenradikale wie Halochinon und Zyanochinon enthalten, molekular in einem passenden Polymer verteilt wurde.

8. Halbleiterspeicherbauelement nach Anspruch 5, in dem das Ionenradikal-Polymer ein Polymer ist mit heterozyklischen Kationenradikalen, welche Stickstoff und/oder Schwefel in ihrem Seitenstrang oder Hauptstrang enthalten.

9. Halbleiterspeicherbauelement nach Anspruch 4, in dem die polymerische Verbundschicht einen Clathrat-Verbund oder einen Polyion-Komplex mit einem beweglichen Dotierstoff bildet.

10. Halbleiterspeicherbauelement nach Anspruch 9, in dem der Ionclathrat-Verbund wie ein Kronenether oder ein Polyäthylenoxid aufgebaut ist.

11. Halbleiterspeicherbauelement nach Anspruch 4, in dem die elektronenkonjugiert-polymerische Halbleiterschicht (3) und die dotierstoffzurückhaltende Schicht (4) durch eine dotierstoffdurchdringende Schicht getrennt werden.

12. Halbleiterspeicherbauelement nach Anspruch 11, in dem die erste Gate-Elektrode (5) auf der dotierstoffzurückhaltenden Schicht (4) ausgebildet ist, wobei die Isolierschicht (6-1) dazwischen angeordnet ist, und eine zweite Gate-Elektrode (11) auf der elektronenkonjugiert-polymerischen Halbleiterschicht (3) angeordnet ist, wobei eine Isolierschicht (6) dazwischen angeordnet ist.

13. Halbleiterspeicherbauelement nach Anspruch 12, in dem die zweite Gate-Elektrode (11) ein Halbleitersubstrat ist.

14. Halbleiterspeicherbauelement nach einem der Ansprüche 1 bis 13, in dem die erste Gate-Elektrode (5) mit einer der Elektroden des Elektrodenpaares (1, 2) kurzgeschlossen ist.

15. Steuerverfahren für das Halbleiterspeicherbauelement nach den Ansprüchen 1 bis 13, mit dem Schritt, das Speicherbauelement zu programmieren oder zurückzusetzen, durch Anlegen eines positiven oder negativen Spannungsimpulses an die erste Gate-Elektrode, um die Dotierstoffverteilung der elektronenkonjugiert-polymerischen Halbleiterschicht zu verändern und somit deren elektrische Leitfähigkeit zu variieren; Auslesen des Speicherbauelementes durch Anlegen eines Erdpotentials an die erste Gate-Elektrode und Anlegen einer Spannung zwischen dem Elektrodenpaar.

16. Steuerverfahren für das Halbleiterspeicherbauelement nach Anspruch 14, mit den Schritten, das Speicherbauelement zu programmieren oder zurückzusetzen, durch Anlegen eines positiven oder negativen Spannungsimpulses zwischen dem Elektrodenpaar, um die Dotierstoffverteilung in der elektronenkonjugiert-polymerischen Halbleiterschicht zu verändern und somit die elektrische Leitfähigkeit derselben zu variieren; Auslesen des Speicherbauelementes durch Anlegen einer Spannung zwischen dem Elektrodenpaar, welche eine kleinere Amplitude aufweist als die des Spannungsimpulses.

Revendications

1. Dispositif de mémoire à semi-conducteur ayant une structure MISFET comprenant une couche semi-conductrice polymère conjugué d'électrons (3) contenant un dopant mobile pour communiquer une conductivité électrique formée entre une paire d'électrodes (1, 2) et au moins une première électrode de grille (5) placée entre ladite paire d'électrodes (1,2) avec une couche d'isolation (6) ou une couche de résistance élevée interposée le long de ladite couche semi-conductrice polymère conjugué d'électrons (3) de sorte qu'une distribution de dopant dans ladite couche semiconductrice polymère conjugué d'électrons (3) est commandée par ladite première électrode de grille (5) pour commander la conductivité électrique d'un canal conducteur se composant de ladite couche semiconductrice polymère conjugué d'électrons.

2. Dispositif de mémoire à semi-conducteur selon la

revendication 1, dans lequel la couche semi-conductrice polymère conjugué d'électrons (3) comprend un dopant pour communiquer une conductivité électrique, un polymère ayant une longue chaîne d'électrons principale de conjugué de forme π, et un plastifiant dissolvant ledit dopant.

3. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel la couche semi-conductrice polymère conjugué d'électrons (3) est au moins d'un type sélectionné parmi le polythiophène, polypyrrole, poly-p-phénylène, polymérisés électrolytiquement et leurs copolymères et dérivés.

4. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel la couche semi-conductrice polymère conjugué d'électrons (3) est formée au voisinage de la couche (4) de retenue de dopant se composant d'une couche de composé polymère complexé avec ledit dopant mobile ou d'un radical ionique contenu dans un composé polymère comprenant ledit dopant mobile.

5. Dispositif de mémoire à semi-conducteur selon la revendication 4, dans lequel le radical ionique contenu dans un composé polymère comprend au moins un type sélectionné parmi
   (a) un composé polymère conjugué d'électrons de faible conductivité contenant un dopant mobile,
   (b) un composé polymère dans lequel un sel dérivé d'un dopant mobile et d'un radical ionique inversement polaire est dispersé ;
   (c) un complexe polymère d'un dopant mobile et d'un polymère de radical ionique, et
   (d) un composé de faible conductivité fait d'un dopant mobile contenu dans un polymère conjugué d'électrons de haute conductivité et un polymère d'isolation.

6. Dispositif de mémoire à semi-conducteur selon la revendication 5, dans lequel le dopant contenu dans un composé polymère conjugué d'électrons de faible conductivité comprend un polymère ayant une chaîne latérale conjugué d'électrons en forme de π ou un polymère n'ayant pas de chaîne principale conjugué d'électrons de longue distance de celui-ci.

7. Dispositif de mémoire à semi-conducteur selon la revendication 5, dans lequel le composé polymère dans lequel un sel constitué d'un dopant mobile et d'un radical ionique inversement polaire est dispersé, comprend un sel ayant, comme radicaux ioniques, des radicaux cationiques hétérocycliques contenant de l'azote et/ou du soufre ou des radicaux à anionique tels que l'aloquinone et le cyanoquinone a été dispersé de façon moléculaire dans un polymère compatible.

8. Dispositif de mémoire à semi-conducteur selon la revendication 5, dans lequel le polymère à radical ionique est un polymère ayant des radicaux cationiques hétérocycliques contenant de l'azote et/ou du soufre dans sa chaîne latérale ou sa chaîne principale.

9. Dispositif de mémoire à semi-conducteur selon la revendication 4, dans lequel la couche de composé polymère forme un composé de clathrate ionique ou un complexe polyionique avec un dopant mobile.

10. Dispositif de mémoire à semi-conducteur selon la revendication 9, dans lequel le composé de clathrate ionique est d'une construction d'éther crown ou d'oxyde de polyéthylène.

11. Dispositif de mémoire à semi-conducteur selon la revendication 4, dans lequel la couche semi-conductrice polymère conjugué d'électrons (3) et la couche de retenue de dopant (4) sont séparées par une couche de pénétration de dopant.

12. Dispositif de mémoire à semi-conducteur selon la revendication 11, dans lequel ladite première électrode de grille (5) est formée sur ladite couche de retenue de dopant (4) avec ladite couche isolante (6-1) interposée entre elles, et une seconde électrode de grille (11) est placée sur ladite couche semi-conductrice polymère conjugué d'électrons (3) avec une couche isolante (6) interposée entre elles.

13. Dispositif de mémoire à semi-conducteur selon la revendication 12, dans lequel la seconde électrode de grille (11) est un substrat semi-conducteur.

14. Dispositif de mémoire à semi-conducteur selon l'une quelconque des revendications 1 à 13, dans lequel la première électrode de grille (5) est court-circuitée par une électrode de ladite paire d'électrodes (1, 2).

15. Procédé de commande pour le dispositif de mémoire à semi-conducteur selon les revendications 1 à 13, comprenant l'étape de programmation ou de réinitialisation du dispositif de mémoire en appliquant une impulsion de tension positive ou négative à la première électrode de grille pour changer la distribution de dopant de ladite couche semi-conductrice polymère conjugué d'électrons, faisant varier ainsi la conductivité électri-

que de celle-ci ; de lecture dudit dispositif de mémoire en appliquant un potentiel de masse à ladite première électrode de grille et en appliquant une tension entre ladite paire d'électrodes.

16. Procédé de commande pour le dispositif de mémoire à semi-conducteur selon la revendication 14, comprenant les étapes de programmation ou de réinitialisation du dispositif de mémoire en appliquant une impulsion de tension positive ou négative entre ladite paire d'électrodes pour changer la distribution de dopant de ladite couche semi-conductrice polymère conjugué d'électrons, faisant varier ainsi la conductivité électrique de celle-ci; lecture dudit dispositif de mémoire en appliquant une tension entre ladite paire d'électrodes ayant une amplitude plus petite que celle de ladite impulsion de tension.

Fig. 1

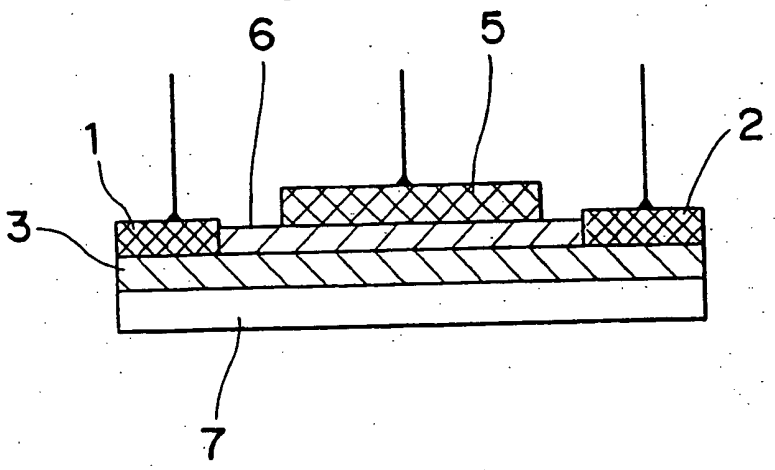


Fig. 2

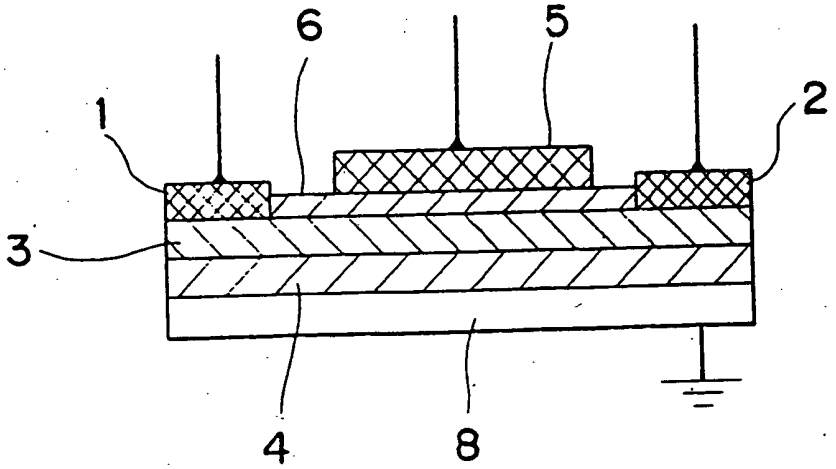


Fig.3

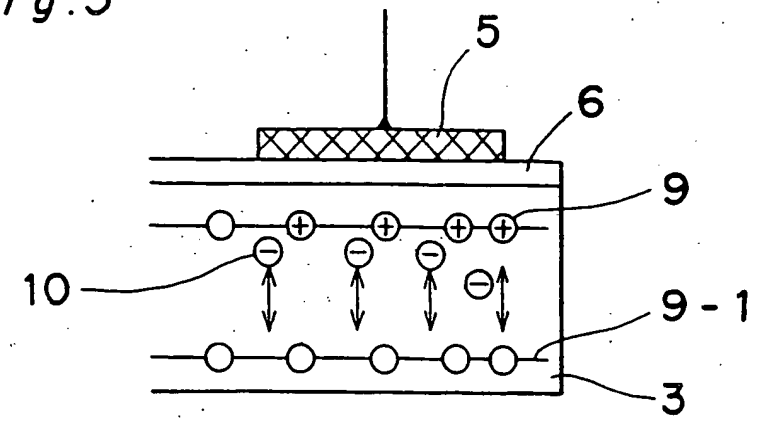
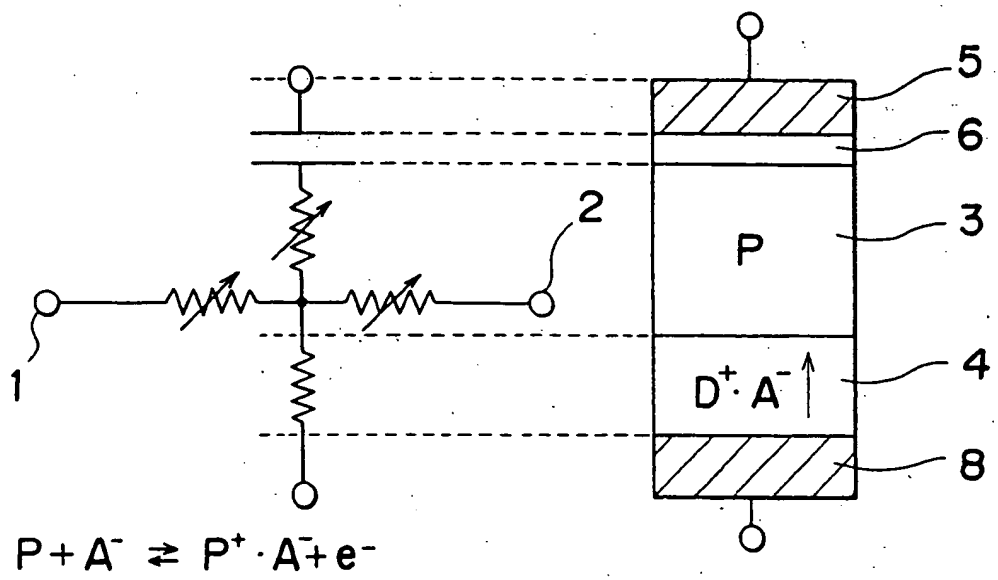


Fig.4



$P + A^- \rightleftarrows P^+ \cdot A^- + e^-$

$D^+ \cdot + e^- \rightleftarrows D^\circ$

Fig.5

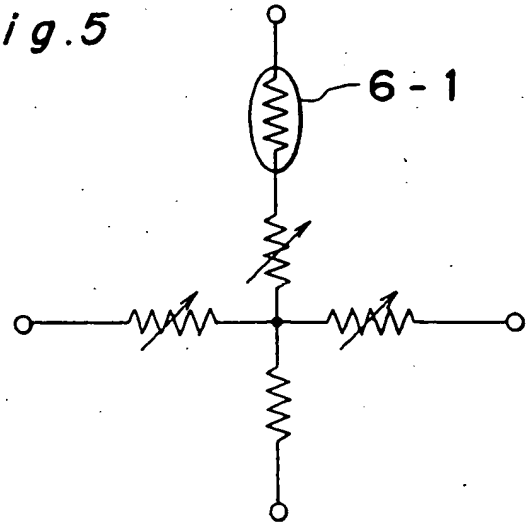


Fig. 6

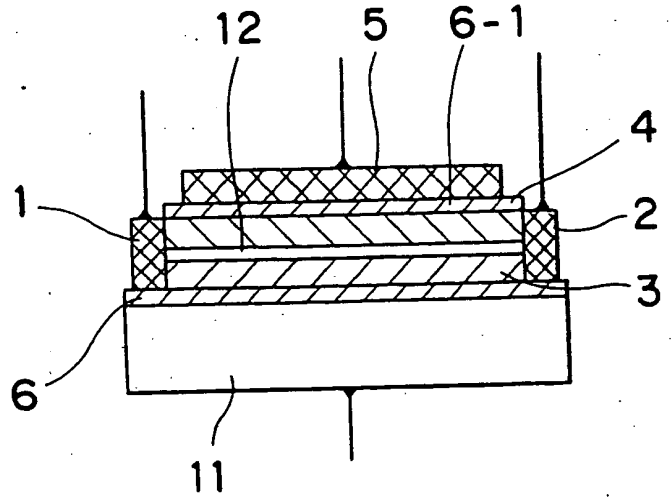


Fig. 7

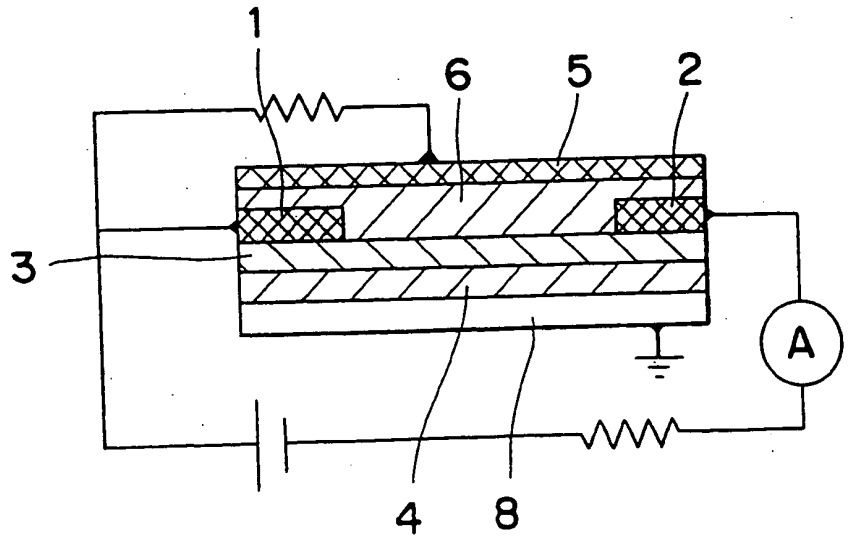


Fig. 8

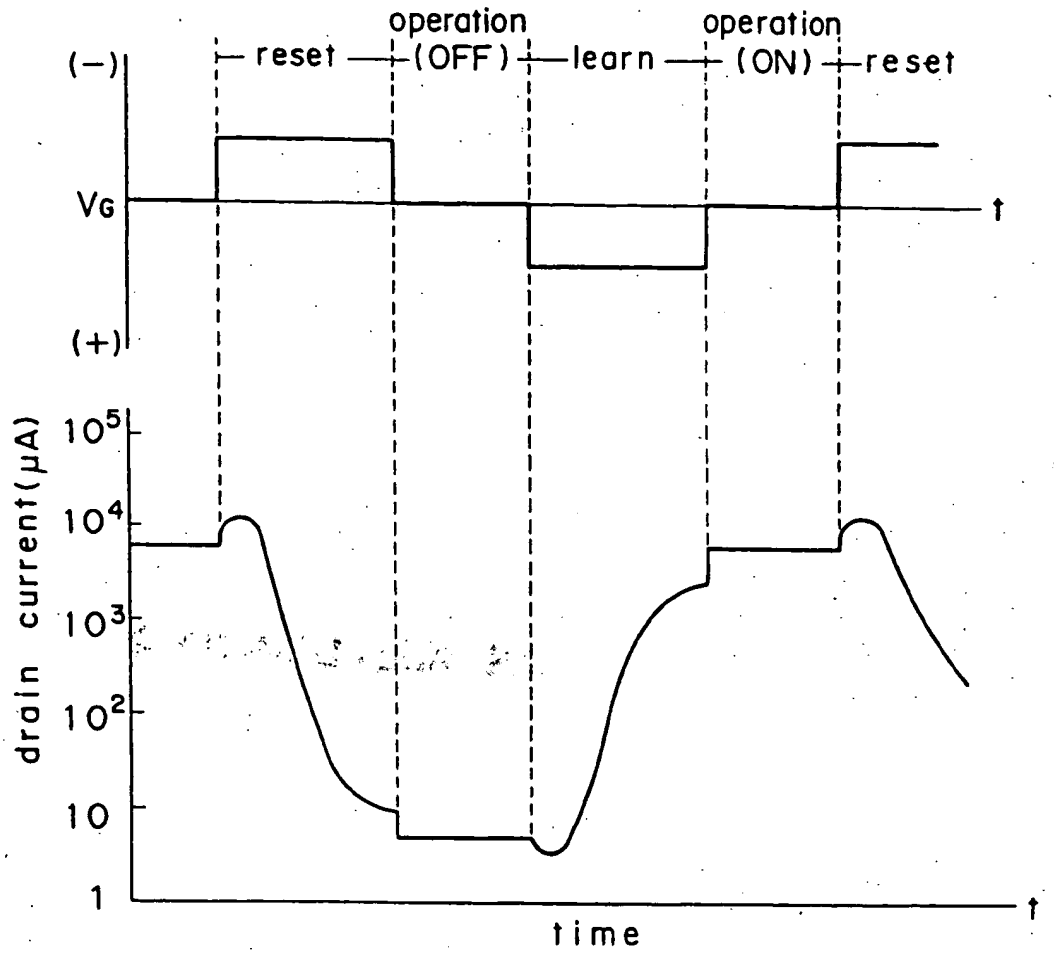


Fig. 9

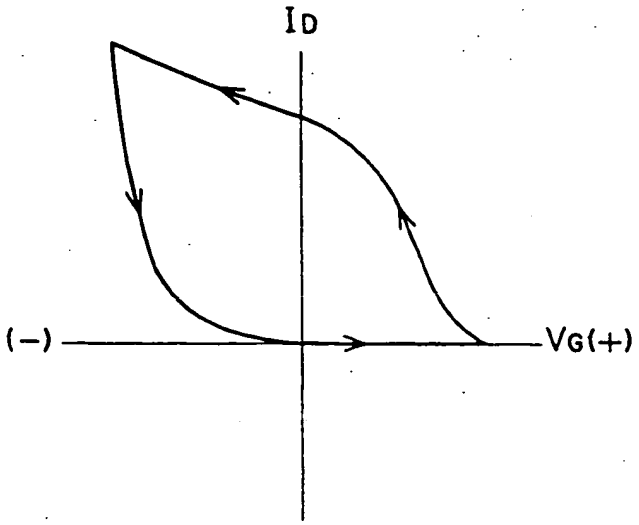


Fig. 10